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PROSECUTION OF THE SUBJECT APPLICATION

Applicants: T. Hironaka et al. Attorney Docket No. SUSU121842
Application No.: Filed Concurrently Herewith Group Art Unit: ---
Filed: Concurrently Herewith Examiner: ---
Title: MULTI-PORT INTEGRATED CACHE

OTHER INFORMATION
(Including Author, Title, Date, Pertinent Pages, Etc.)

*Examiner Cite
Initial No.

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- | | | |
|-------|----|--|
| _____ | O1 | Mattausch, H.J., et al., "Area-Efficient Multi-Port SRAMs for On-Chip Data-Storage with High Random-Access Bandwidth," <i>IEICE Transactions on Electronics E84-C</i> (3):410-417, 2001. |
| _____ | O2 | Mattausch, H.J., and K. Yamada, "Application of Port-Access-Rejection Probability Theory for Integrated N-Port Memory Architecture Optimisation," <i>Electronics Letters</i> 34(9):861-862, 1998. |
| _____ | O3 | Mattausch, H.J., "Hierarchical Architecture for Area-Efficient Integrated N-Port Memories with Latency-Free Multi-Gigabit Per Second Access Bandwidth," <i>Electronics Letters</i> 35(17):1441-1443, 1999. |
| _____ | O4 | Tatsumi, Y., and H.J. Mattausch, "Fast Quadratic Increase of Multiport-Storage-Cell Area with Port Number," <i>Electronics Letters</i> 35(25):2185-2187, 1999. |

Examiner

Date Considered

*Examiner: Initial if reference considered, whether or not citation is in conformance with M.P.E.P. § 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

JMS:snh

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